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# COMPLIANT PASSIVATED EDGE SEAL FOR LOW-K INTERCONNECT STRUCTURES

## Abstract

A structure for a chip or chip package is disclosed, with final passivation and terminal metallurgy which are mechanically decoupled but electrically coupled to the multilayer on-chip interconnects. This decoupling allows the chip to survive packaging stresses in the final passivation region, with strain relief from the decoupling region and compliant leads therein, so that on-chip interconnect levels do not feel these external packaging or other stresses. This structure is particularly preferred for on-chip interconnects consisting of Cu and low-k dielectric, the latter having inferior mechanical properties relative to $SiO_2$. The decoupled region extends over all chips on the wafer. It may also extend into the edgeseal or dicing channel region so as to allow chip dicing and retention of this mechanical decoupling all around every chip on the wafer.